
competing requirements, the demands on the process for fabricating the device are becoming more stringent. Conventionally, devices are formed on a wafer of silicon substrate. Electrical devices such as transistors are formed by well-known processing steps in an attempt to achieve maximum integration of the device to the extent permitted by the particular device. Next, a dielectric layer is formed on the wafer. The dielectric layer is then patterned by a photolithographic process to form an opening. Then, the dielectric layer is etched to remove part of the dielectric layer to a depth that exposes an underlying region of the wafer and leave some dielectric material within the opening. This is followed by formation of an electrically conductive material into the opening, for example, by a blanket or conformal deposition of a conductive material into the opening followed by a chemical-mechanical polishing step to remove excessive conductive material from the dielectric layer surface and to provide a planarized surface. However, there is an increasingly difficult problem in incorporating buried trench capacitors in a high performance DRAM device. This problem is particularly difficult at device nodes having a 0.25 μm or less spacing. To provide adequate capacitance for such devices, an area of the wafer surface must be given over to the

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